IN THE CLAIMS

Please amend claims 1, 6, 8, 11, 15-18, 21, 23, 28, 30, and 32, cancel claims 2, 3, 7, 9, 10, 13, 14, 19, 20, and 22, and add new claims 33-42 as set forth below. All currently pending claims and status indicators have been reproduced below. This listing will replace all previous versions of the claims.

1. (currently amended) A method for forming polymer within a reaction chamber, the process comprising:

providing a reaction chamber;

introducing a polymer-forming gas within the reaction chamber concurrent with etching of a photoresist layer of a first semiconductor wafer in the reaction chamber; and

regulating an environment within the reaction chamber to form a polymer on an interior surface of the reaction chamber.

2-3. (canceled)

4. (original) The method of claim 1, wherein the environment within the reaction chamber comprises a temperature range between about 90°C and 250°C.

5. (original) The method of claim 1, wherein the environment within the reaction chamber comprises a pressure range between about 0mT to about 200mT.

6. (currently amended) The method of claim 1, wherein the provided polymer-building gas comprises at least one of:

difluoromethane;

trifluoromethane;

octofluorocyclobutane; ~~and~~ or

hexafluoro-13 butadiene, or any combination thereof.

7. (canceled)

8. (currently amended) A method of manufacturing an integrated circuit, the method comprising the acts of:

disposing a first semiconductor wafer having a plurality of layers in a reaction chamber;

processing the first semiconductor wafer in the reaction chamber, the processing including etching a photoresist layer of the first semiconductor wafer; and

reducing the standard deviation of the critical dimensions of the first semiconductor wafer by providing a polymer-building gas in the reaction chamber during the etching of the photoresist layer of the first

semiconductor wafer to create a layer of polymer on an interior portion of the reaction chamber.

9-10. (canceled)

11. (currently amended) The method of claim 8, wherein the provided polymer-building gas comprises at least one of:

difluoromethane;

trifluoromethane;

octofluorocyclobutane; ~~and~~ or

hexafluoro-13 butadiene, or any combination thereof.

12. (original) The method of claim 8, wherein the polymer-building gas is provided in a relatively small ratio as compared with a reactant gas.

13-14. (canceled)

15. (currently amended) The method of claim 8 ~~14~~, wherein at least one layer of the first ~~layered~~ semiconductor wafer was formed through deposition.

16. (currently amended) The method of claim 8 ~~14~~, wherein the first ~~layered~~ semiconductor wafer comprises at least one of:

an oxide layer; or

an anti-reflective coating~~; and~~

~~a photoresist layer~~, or any combination thereof.

17. (currently amended) The method of claim 8, wherein processing the first semiconductor wafer in the reaction chamber comprises ~~at least one of:~~

layering the first semiconductor wafer~~; and~~

~~patterning the semiconductor wafer~~.

18. (currently amended) The method of claim 17, wherein layering the first semiconductor wafer comprises at least one of:

depositing material on the first semiconductor wafer; ~~and~~ or

growing material on the first semiconductor wafer, or any combination thereof.

19-20. (canceled)

21. (currently amended) The method of claim 8 ~~20~~, wherein etching the photoresist layer of the first semiconductor wafer comprises plasma etching of the photoresist layer.

22. (canceled)

23. (currently amended) A method of manufacturing an electronic device, the method comprising:

providing an integrated circuit manufactured by a process comprising:

disposing a first semiconductor wafer in a reaction chamber;

processing the first semiconductor wafer in the reaction chamber; and

providing a polymer-building gas in the reaction chamber during etching of a photoresist layer of the first semiconductor wafer to create a layer of polymer on an interior portion of the reaction chamber;

packaging the integrated circuit; and

electrically coupling the integrated circuit to a substrate.

24. (original) The method of claim 23, wherein a plurality of integrated circuits are electrically coupled to the substrate.

25. (original) The method of claim 23, wherein the substrate comprises a circuit board.

26. (original) The method of claim 23, wherein the electronic device comprises a memory device.

27. (original) The method of claim 23, wherein the electronic device comprises a DIMM.

28. (currently amended) A method of manufacturing an electronic system, the method comprising:

providing an integrated circuit manufactured by a process comprising:

disposing a first semiconductor wafer in a reaction chamber;

processing the first semiconductor wafer in the reaction chamber; and

providing a polymer-building gas in the reaction chamber during etching of a photoresist layer of the first semiconductor wafer to create a layer of polymer on an interior portion of the reaction chamber; and

incorporating the integrated circuit into an electronic device.

29. (original) The method of claim 28, wherein the electronic system comprises a processor based system.

30. (currently amended) The method of claim 29, wherein the processor based system comprises at least one of:

a computer;

a pager;

a cellular communication device;

a personal organizer; ~~and~~ or

a control circuit, or any combination thereof.

31. (original) The method of claim 28, wherein at least one peripheral device is attached to the electronic system.

32. (currently amended) The method of claim 31, wherein the at least one peripheral comprises at least one of:

a user interface;

a display; ~~and~~ or

an antenna, or any combination thereof.

33. (new) The method of claim 1, comprising:

removing the first semiconductor wafer from the reaction chamber;

inserting a second semiconductor wafer into the reaction chamber; and

etching the second semiconductor wafer, wherein the polymer formed on the interior surface of the reaction chamber reduces the standard deviation of the critical dimensions of the second semiconductor wafer.

34. (new) The method of claim 33, wherein etching the second semiconductor wafer is performed without adding additional polymer-forming gas to the reaction chamber.

35. (new) The method of claim 1, wherein introducing the polymer-forming gas reduces the standard deviation of the critical dimensions of the first semiconductor wafer.

36. (new) The method of claim 1, wherein no additional polymer-forming gas is introduced within the reaction chamber while the first semiconductor wafer is present within the reaction chamber.

37. (new) The method of claim 8, comprising:

removing the first semiconductor wafer from the reaction chamber;

inserting a second semiconductor wafer into the reaction chamber; and

etching the second semiconductor wafer without adding additional polymer-building gas to the reaction chamber, wherein the polymer on the interior surface of the reaction chamber reduces the standard deviation of the critical dimensions of the second semiconductor wafer.

38. (new) The method of claim 8, wherein no polymer-building gas is provided within the reaction chamber during processing of the first semiconductor wafer within the reaction chamber other than the polymer-building gas provided during the photoresist layer etching.

39. (new) The method of claim 23, wherein the integrated circuit manufacturing process comprises:

removing the first semiconductor wafer from the reaction chamber;

inserting a second semiconductor wafer into the reaction chamber; and

etching the second semiconductor wafer without adding additional polymer-building gas to the reaction chamber, wherein the polymer on the interior

surface of the reaction chamber reduces the standard deviation of the critical dimensions of the second semiconductor wafer.

40. (new) The method of claim 23, wherein providing the polymer-building gas reduces the standard deviation of the critical dimensions of the first semiconductor wafer.

41. (new) The method of claim 28, wherein the integrated circuit manufacturing process comprises:

removing the first semiconductor wafer from the reaction chamber;

inserting a second semiconductor wafer into the reaction chamber; and

etching the second semiconductor wafer without adding additional polymer-building gas to the reaction chamber, wherein the polymer on the interior surface of the reaction chamber reduces the standard deviation of the critical dimensions of the second semiconductor wafer.

42. (new) The method of claim 28, wherein providing the polymer-building gas reduces the standard deviation of the critical dimensions of the first semiconductor wafer.